

FIG. 1

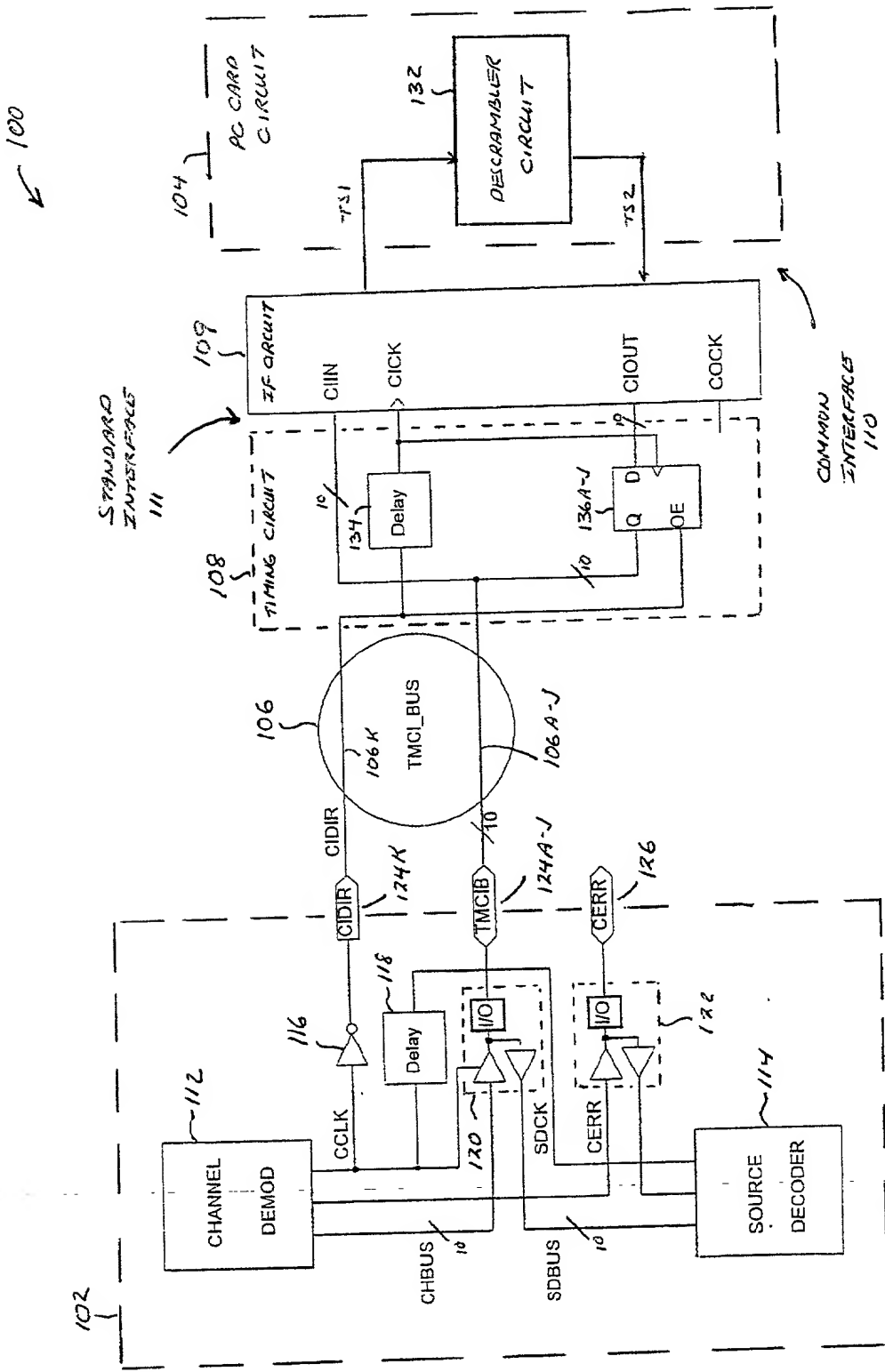


FIG. 2

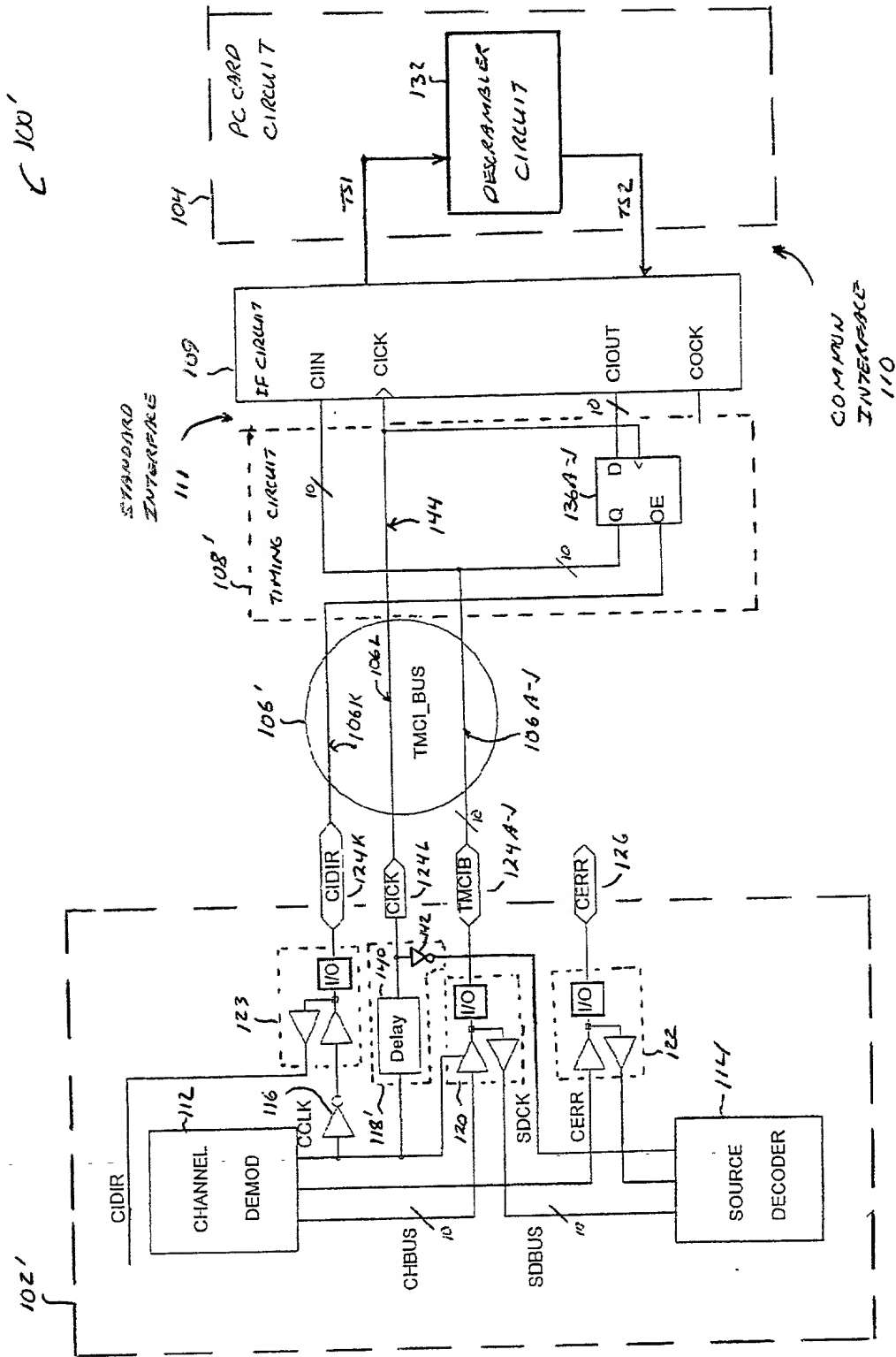


FIG. 3

The timing diagram illustrates the operation of the 68000 microprocessor over a 4,500 ns period. The signals shown are:

- CK27M**: 27 MHz clock signal.
- CCLK**: Core clock signal.
- CDBUS**: Core data bus.
- CIDIR**: Core instruction/data bus direction signal.
- BUSOUT**: Bus output signal.
- DBUS**: Data bus signal.
- CICK**: Core instruction clock signal.
- QBUS**: Queue bus signal.
- QDBUS**: Queue data bus signal.
- BUSIN**: Bus input signal.
- SDCK**: Serial data clock signal.
- SDBUS**: Serial data bus signal.

Key annotations and data values include:

- Address values**: 150, 151, 152, 158, 160, 164, 166, 162.
- Data values**: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C.
- Control signals**: 158, 152, 156, 162.

FIG. 4

